Influence of the Interaction between Antenna Currents and Return Currents on the Coupling between Digital Interfaces and On-Board Antennas

Davy Pissoort[#1], Mehdi Mechaik[*1], Henry Zeng[*2], Charlie Shu[*3], Charles Jackson[*4], Jan Van Hese[†1]

[#] *KU Leuven, Laboratory FMEC ,Reliability in Mechatronics and ICT Research Group*
Zeedijk 101, B8400 Ostend, Belgium
[1] davy.pissoort@khbo.be

[*] *Nvidia Corporation*
2701 San Tomas Expressway, Santa Clara, CA 95050, USA
[1] mmechaik@nvidia.com
[2] hzeng@nvidia.com
[3] cshu@nvidia.com
[4] cjackson@nvidia.com

[†]*Agilent Technologies*
Kortrijksesteenweg 1093B, B9051 Sint-Denijs-Westrem, Belgium
[2] jan_vanhese@agilent.com

***Abstract*—Due to the integration of wireless modules and on-board antennas at printed circuit board (PCB) level, design engineers are faced with even more difficult challenges to avoid intra-system electromagnetic interference issues. When starting to design a printed circuit board, the first rule is to partition the printed circuit board such that noisy components are placed physically far away from sensitive components. This rule relies on the phenomenon that at moderately high frequencies, return currents tend to stay in proximity of and close to their signal currents. Unfortunately, on-board antennas most often induce antenna currents which are distributed over a large part of the PCB's power/ground planes. As a result, significant interference might even happen with circuits which are placed physically far away from the antenna's location. During the whole design process, the engineer has to make sure that the overlap area between the antenna currents and the return currents paths of the critical circuits is as minimal as possible. This is achieved by properly placing circuits, keeping track of the antenna current distribution, and by avoiding all return path discontinuities. "Intuitive" solutions as putting a slot around the critical circuits might actually lead to higher electromagnetic interference levels. Hence, full-wave simulations which allow for visualizing all current distributions and their interactions, are an important asset in aiding the design process. The simulation process becomes a key element in a judicial component placement to minimize the interaction between antenna currents and return currents in PCB designs.**

I. Introduction

Many mobile devices such as smartphones, tablets, portable PCs and others, nowadays have multiple-input-multiple-output (MIMO) on-board antennas. Designing and implementing such on-board wireless modules comprising multi-band antennas make Electro-Magnetic Interference (EMI) issues on printed circuit boards (PCBs) even more complex problems than ever before [1]. Avoiding intra-system EMI or "self-jamming" has become one of the main problems that design engineers have to overcome. Full-wave simulations during the early stages of the PCB design process are crucial for co-designing the printed circuit board with the on-board wireless modules and antennas.

In this paper it will be shown that the overlap between antenna currents induced in PCB ground planes and return currents of critical digital traces is a good indicator for these intra-system interference issues. Important and successful design steps are: to visualize how the antenna currents are distributed in the ground-plane; to put the digital traces in regions where these currents are small for the critical frequencies; and to make sure that there are no return path discontinuities of the digital current loops, which would significantly increase the interference levels.

This paper is organized as follows. Section 2 describes the design challenges that have to be overcome when integrating on-board antennas. Section 3 discusses the interactions between the currents distributions induced by the antenna and the digital traces in the PCB's ground-planes. Section 4 shows a practical example for the influence of return path discontinuities on this type of intra-system interference. Finally, Section 5 draws concluding remarks.

II. Design challenges related to on-board antennas

During the design process of a PCB with on-board antenna, the engineer is faced with two major challenges, which will be described below.

The first challenge is that these antennas have to be small, while still maintaining the required performance. Typical frequencies for which antennas have to be designed are 900

and 1800 MHz (GSM), 1.57 GHz (GPS), 2.4 GHz (Bluetooth, WLAN), and 5 GHz (WLAN). Due to their small physical size, these on-board antennas rely on the existence of a large ground plane on the PCB to aid in their performance [2]. As a result, the ground-plane shape (width, height, slots, holes,…) will have an influence on resonance frequencies and depths. This already makes it necessary to co-design the on-board antenna with the ground-plane. At the same time, antenna currents are induced in a very large part of the ground plane and can cause intra-system EMI problems in regions that are physically far away from the antenna location.

The second challenge is that modern PCBs contain a lot of high speed digital interfaces such as DDR2/3 or IO buses like USB3.0 (Universal Serial Bus) or HDMI (High-Definition Multimedia Interface) which can easily interfere with other parts on the PCB, certainly on-board antennas and their attached circuitry. When looking into more detail at the interference between digital interfaces and on-board antennas, one can conclude that the interference can actually happen in two ways, depending on whether the antenna is in receive or in transmit mode:

- If the antenna is in *receive mode*, it will have to be able to successfully receive and process very small signals. As the induced useful voltages at the antenna ports are typically very small, any noise that is induced at those ports leads to a significant decrease of the sensitivity of the receiver circuit. Hence, in receive mode, care has to be taken that the EMI coupling from the on-board digital circuits to the on-board antennas is kept small.
- If the antenna is in *transmit mode*, it will have to send out with a significant amount of power (e.g. 2 Watt for GSM). This means that there are quite high voltages and currents at the antenna ports which can couple significantly to the digital interfaces thereby increasing bit error rates.

III. Influence of Return Path Discontinuities

One of the first and most important rules to avoid interference on PCB level is to partition the PCB in an intelligent way, such that critical noise sources (e.g. high-speed digital circuits, memories,…) are placed far away from sensitive parts (e.g. analog receivers) [3]. The EMI reduction due to partitioning relies mainly on the physical phenomenon that above a few MHz return currents tend to stay very close to their signal current path, thereby minimizing the total current path's inductance. So, as long as this return current path is not disturbed, all currents will be very "local" on the specified part of the PCB and will not interfere heavily with components at other places on the PCB.

Unfortunately, on-board antennas can induce significant antenna currents in a large part of the PCB's ground planes, even in regions that are physically far away from the antenna. For successful partitioning of the PCB, the design engineer has to know the distribution of these antenna currents. During the placement stage of components on the PCB, the design engineer has to carefully select places where the digital interfaces will be placed, keeping in mind the antenna current profiles. Moreover, current path discontinuities have to be avoided. Simply stated, the design engineer has to make sure that there is as little as possible overlap between the antenna currents and the return paths of his digital interfaces. More overlap means a higher level of intra-system interference and visa versa.

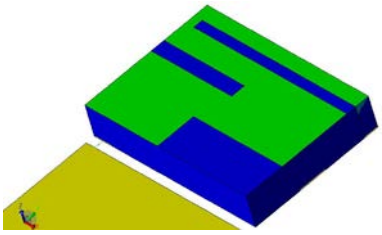


Fig. 1. Multiband on-board monopole antenna

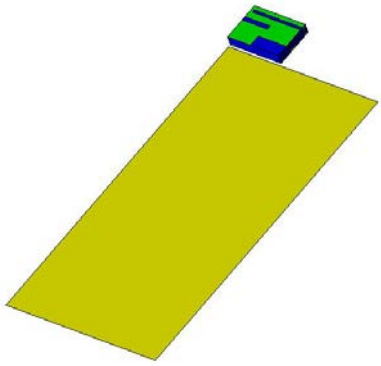


Fig. 2. System under study

IV. Practical Example

In this section, the influence of the interaction between antenna currents on the PCB's ground-plane and a digital interface's return current paths is quantified by means of full-wave simulations. All simulations below are done with the CUDA enabled Finite-Difference Time-Domain (FDTD) solver that is included in Agilent Technologies' 3D EM platform EMPro [4]. The full-wave FDTD method [5] is very suitable for characterizing complex boards for wideband applications. As a time-domain solver it has the advantage that it can capture both broadband (e.g. S-parameters) and steady-state results (e.g. current distributions and radiation patterns) in one single simulation run.

The on-board antenna used as an example in this paper is a folded, multiband planar monopole antenna whose design is inspired by the antenna described in [6]. The design requirements were that the antenna should have good performance around 900 MHz and from 1.7 GHz up to 2.5 GHz. Moreover, it should fit within a volume of 20.0 mm by 8.0 mm by 4.0 mm. These are typical requirements for on-board antennas. The antenna geometry is shown in Fig. 1. The permittivity of the blue material supporting the antenna metallizations is 2.2.

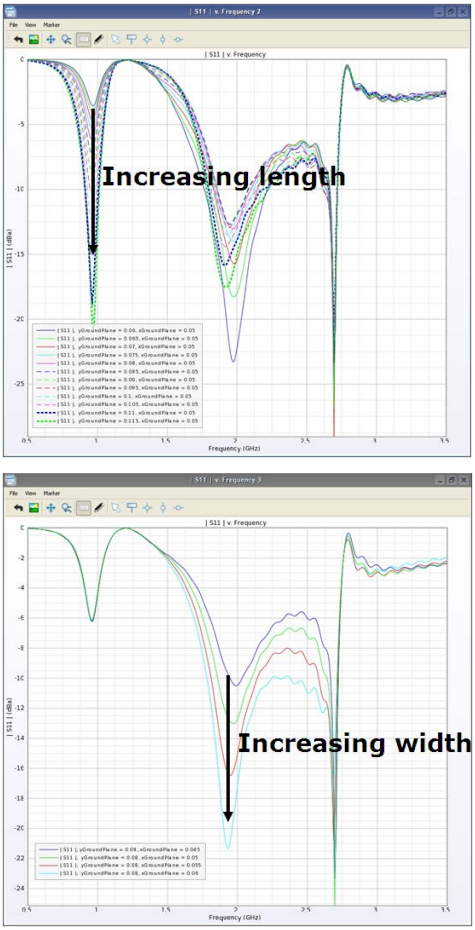


Fig. 3. Influence of the PCB's length (top) and width (bottom) on the return loss of the folded monopole antenna shown in Fig. 1.

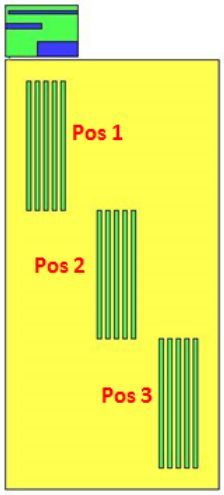
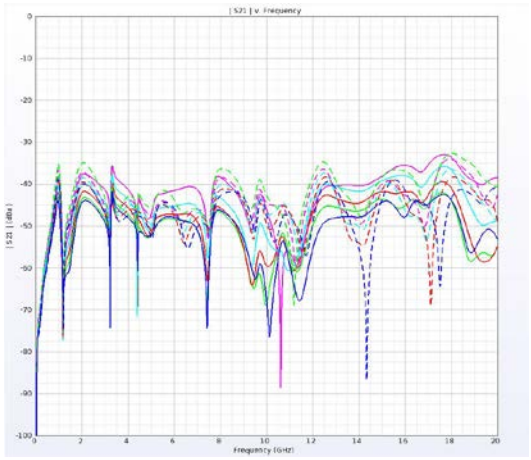
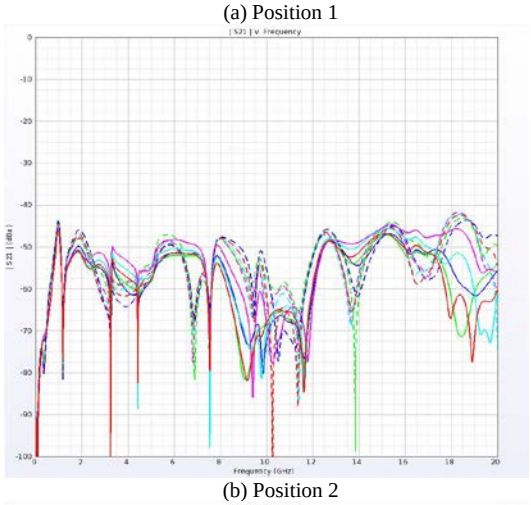


Fig. 4. Digital interfaces on top full ground-plane at three different positions.

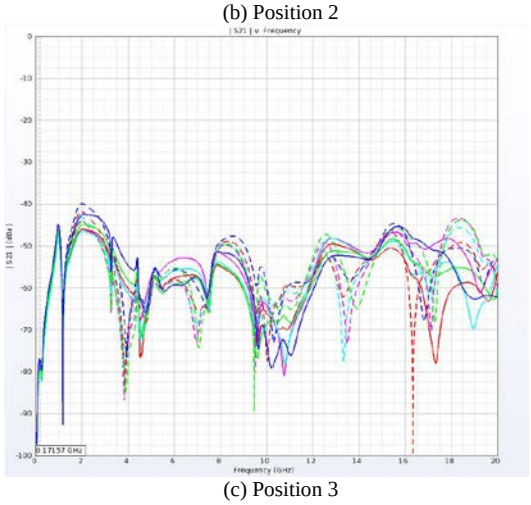
This antenna is mounted at the top left corner of a single-layer PCB (Fig. 2). For such a small antenna, it is known that its performance depends heavily on the ground-plane's size and shape. Fig. 3 shows the influence of the ground-plane's length and width on the return loss of this antenna between 500 MHz and 3.5 GHz, the frequency range of interest for the antenna itself. Increasing the length of the ground-plane affects resonance at 900MHz and 1.9GHz. A larger ground-plane results in stronger resonance mostly at low and mid-frequencies and generally improves reflections. Increasing the width of the ground-plane seems to affect mid frequencies (1.9GHz) only. In the remainder of this paper, the ground-plane size is taken as100 mm by 50 mm.



(a) Position 1



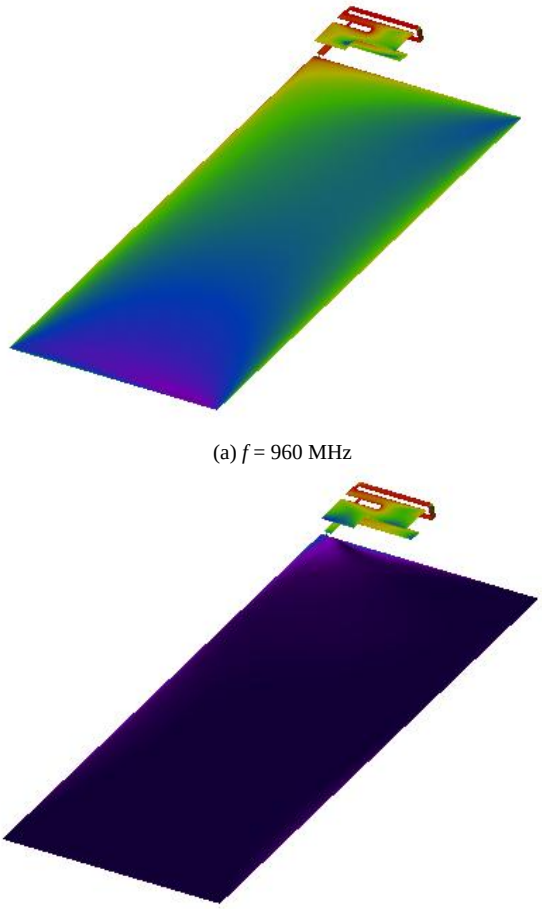
(b) Position 2



(c) Position 3

Fig. 5. Coupling ($|S_{21}|$) from antenna to digital interface in Fig. 4.

Fig. 4 shows the first test-case that will be used to quantify the correlation between the induced antenna currents and the coupling between digital interfaces and the on-board antenna. The digital interfaces are modelled as five parallel 50 Ohm microstrip lines that are 5 cm long and spaced out by about 1 mm. They are positioned at three different locations (close to the antenna, half-way away from the antenna, and far away from the antenna).



(a) f = 960 MHz

(b) f = 1.17 GHz

(b) f = 2.0 GHz

Fig. 6. Antenna current distribution on full ground plane

Fig. 5 shows the coupling for the three positions. Based on distance, one would expect that the coupling is the lowest for the case corresponding to interfaces placed far away from the antenna (position 3). However, this is not the case. For example, at 2 GHz, the coupling between the antenna and the interfaces in position 3 is almost as strong as that between the antenna and the interfaces in position 1.. At 1.17 GHz, the coupling is low for all three cases. These results can be explained by examining the antenna current distributions in the ground-plane for each position. These current distributions are shown in Fig. 6 for 960 MHz (strong coupling), 1.17 GHz (weak coupling) and 2 GHz (strong coupling). Note that (*i*) there can be significant current induced at the lower right side of the ground-plane as is the case for 960MHz and 2GHz frequencies and (ii) at 1.17 GHz there are almost no currents induced in the ground-plane, where most of the current stays local to the antenna.

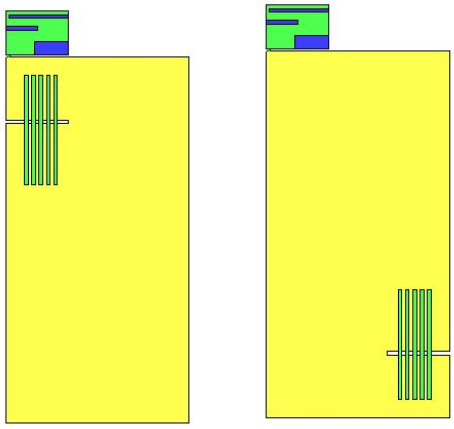


Fig. 7. Digital interfaces crossing a slot in the ground-plane (left: close to antenna; right: far away from antenna).

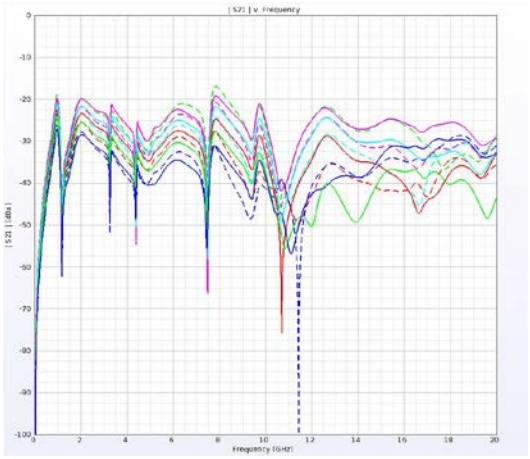
Fig. 7 shows the second test-case that will be used to quantify the influence of return path discontinuities on the coupling between digital interfaces and the on-board antenna. The traces are routed over a slot in the ground plane.

Fig. 8 shows the coupling for the two positions shown in Fig. 7. When comparing to Fig. 5, one notices an increase of the coupling more than 15dB for both cases. The antenna current distributions given in Fig.9 (at 2 GHz), show that the slot "pushes" the antenna currents to the inner part of the PCB. Moreover, the slot will also alter the current distribution of the traces' return currents thereby increasing their inductance. These two effects lead to an increased coupling.

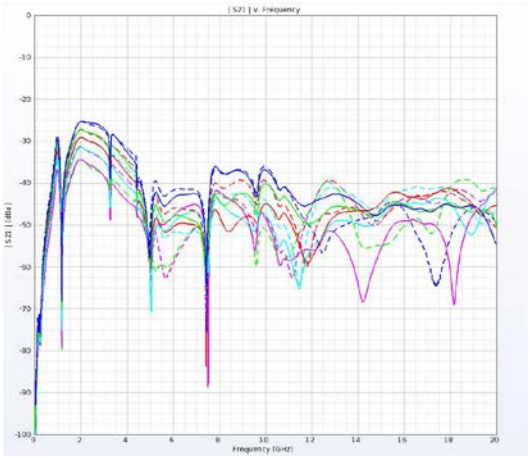
Based on the above results, it is clear that one needs to try to keep the antenna currents away from the area in the ground-plane close to the digital traces. As a result, one could be tempted to put e.g. a slot completely around the traces, as shown in Fig. 10.

Unfortunately, Fig. 11 shows that this reasoning is not correct. In both cases, the slot around the traces actually leads to a

higher coupling.Again, this can be understood based on the current distributions in the ground-plane which are shown in Fig. 12 for 2.36 GHz. The slot does not shield the traces completely from coupling.

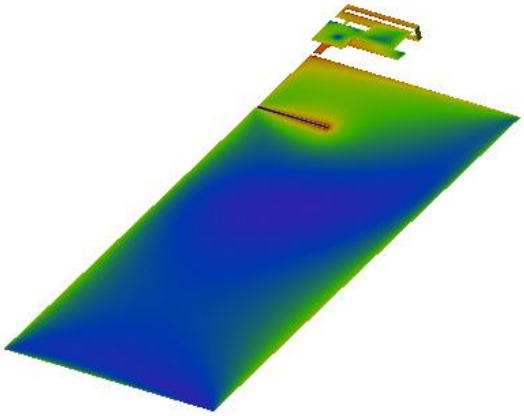


(a) Close to antenna

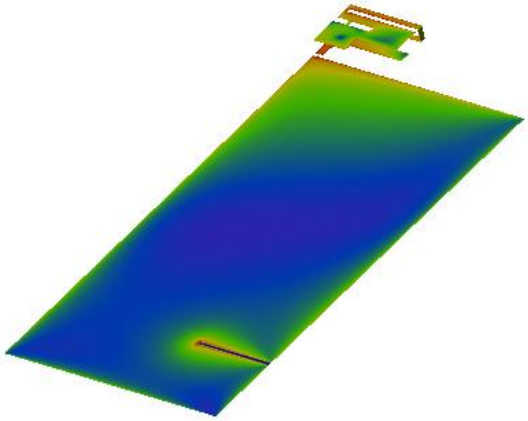


(b) Far away from antenna

Fig. 8. Coupling ($|S_{21}|$) from antenna to digital interfaces that are route over a slot in the ground plane.



(a) Slot close to antenna



(b) Slot far away from antenna

Fig. 9. Antenna current distribution at 2 GHz on ground-plane with slot

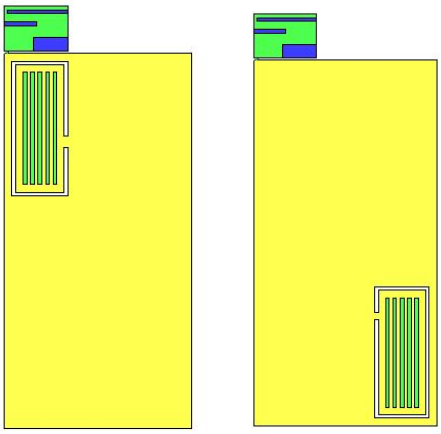
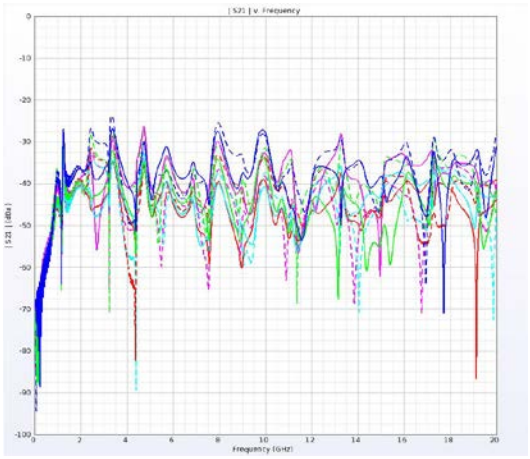
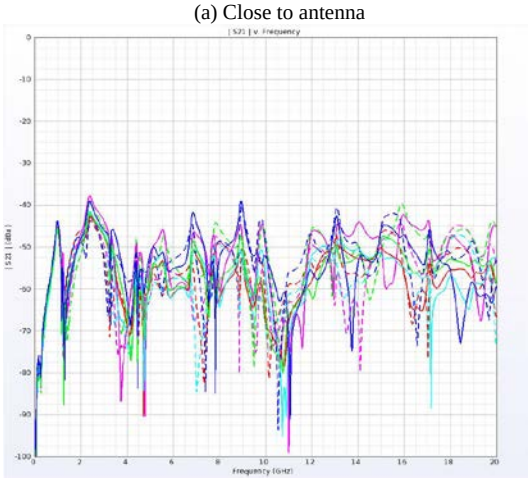


Fig. 10. Digital interfaces surrounded by a slot in the ground-plane (left: close to antenna; right: far away from antenna).



(a) Close to antenna

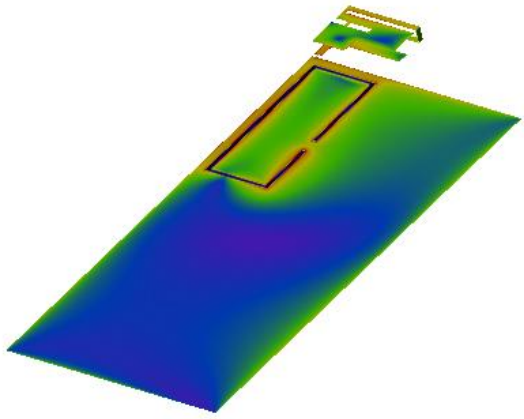


(b) Far away from antenna

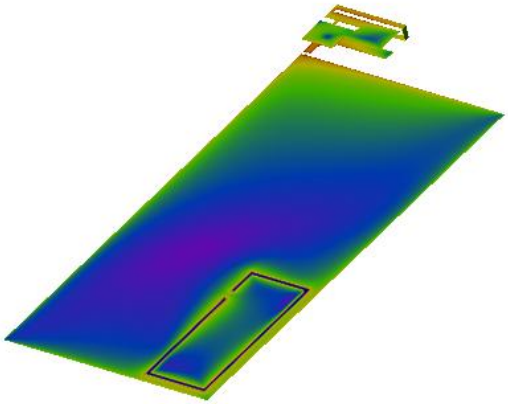
Fig. 11. Coupling ($|S_{21}|$) from antenna to digital interfaces that are surrounded by a slot in the ground plane.

V. Conclusion

On-board antennas very often induce antenna currents which are distributed over a large part of the printed circuit board's power/ground planes. Significant interference might even happen with circuits which are physically far away from the antenna's location. During the whole design process, the engineer has to make sure that the overlap between the antenna currents and the return currents paths of the critical circuits is as minimal as possible. This is achieved by proper location of the circuits, keeping in mind the antenna current distribution, and by avoiding all return path discontinuities. "Intuitive" solutions as putting a slot completely around the critical circuits does not lead to perfect shielding of electromagnetic interference levels and could increase coupling for some cases



(a) Slot close to antenna



(b) Slot far away from antenna

Fig. 12. Antenna current distribution at 2.36 GHz on ground-plane with slot surrounding area of digital interfaces.

References

[1] B. Archambeault, C. Brench, and S. Connor, "Review of Printed Circuit Board Level EMI/EMC Issues and Tools", *IEEE Trans. Electromagn. Compat.*, May 2010, pp. 455-461.

[2] M.C. Hynch and W. Stutzman, "Ground Plane Effects on Planar Inverted F Antenna (PIFA) Performance", *IEEE Proc. Microw. Antennas Propag.*, 2003, pp. 209-213.

[3] H. Ott, "*Electromagnetic Compatibility Engineering*", Wiley, 2009.

[4] Agilent Technologies, Agilent EMPro, available from: http://www.home.agilent.com/

[5] A. Taflove and S. C. Hagness, Computational Electrodynamics: The Finite-Difference Time-Domain Method, 3rd ed., Artech House, 2005.

[6] R.A. Bhatti and S.O. Park, "Internal Multiband Monopole Antenna for Modern Multifunctional Mobile Phones", *Proc. of IBCAST*, 2009, pp. 93-95.