16.5 A Flexible Thin-Film Pixel Array with a Charge-to-Current Gain of 59μA/pC and 0.33% Nonlinearity and a Cost Effective Readout Circuit for Large-Area X-ray Imaging

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We report an active, medical-grade, high resolution, high dynamic range X-ray backplane based on a-IGZO thin-film technology with fast readout. This enables low dose, video rate X-ray imaging. Fast X-ray imaging will find its applications not only in medical, but also in non-destructive inspection. Curved imagers will yield sharper images when illuminated from a point source. This has been achieved thanks to superior a-IGZO technology and a pixel topology that improves noise performance and allows a cost-effective external readout.

Obtaining a lower X-ray dose for medical imaging has long been a research topic of interest and profound relevance. For large-area digital imaging (chest X-ray, mammography, etc.), technology has been limited to flat panel display technology (FPD) on glass using a-Si for cost reasons. a-Si has severely limiting properties: n-type only, low mobility, and high bias stress. Only a passive pixel scheme with one access transistor per pixel can be used, which imposes tough specs on the external readout ICs (ROICs). Our modified pixel design approach leads to relaxed specification for the ROIC without compromising performance, resulting in a more cost-effective X-ray imager.

a-IGZO is a thin-film technology which greatly increases the possible applications compared to a-Si. Mobility, speed, stability and variability are all improved, which allows for the active amplification of the signal within each pixel. Our backplane technology supports critical dimensions (CD) down to 3μm. However, the classical CD for display technologies of 5μm leads to a better uniformity and yield. Therefore we also report the performance of a pixel with CD = 5μm. Details about our a-IGZO self-aligned (SA) technology can be found in Fig. 16.5.1 [1].

Active amplification within pixel increases both the speed and the dynamic range of a pixel by buffering and reducing dataline noise. Due to the low mobility and large dataline capacitance, the thin-film active pixels (APS) operate in a current mode [2]. A few papers have already presented the first steps using an APS [3] [4] [5]. The main goal of a current-mode active pixel is to convert the incoming signal, i.e. the charges generated by the photodiode, into a current that can be read out by the ROIC. Therefore, the most important figure of merit is the charge-to-current gain (CtC gain), $\Delta I_{out}/\Delta Q_{in}$, the ratio between the increase of the output current divided by the change in charge on the pixel capacitor. We achieve measured CtC gains of up to 59μA/pC, a factor 137 better than state-of-the-art as described by Karim et al [3]. A die micrograph can be found in Fig. 16.5.7. For a fixed pixel size, the CtC gain can be increased by decreasing the minimal transistor length of the technology. By going from critical dimension (CD) 5μm to 3μm, the CtC gain can be increased from 27μA/pC to 59μA/pC. The transfer curve of the pixels demonstrating this is shown in Fig. 16.5.3.

Increasing CtC gain comes at a cost: improvements in gain will introduce a reduction in linearity. Non-linearity is however only a secondary parameter since for most applications, further steps will implement non-linear operations on the image to improve certain image properties, like sharpness or contrast. Using a quadratic interpolation, the resulting output linearity can be increased. The added cost is limited, because a zero-point and gain calibration is required to compensate for variability and degradation anyhow. For a pixel with CD=3μm, the maximum remaining non-linearity after quadratic compensation is 0.33%. For a 5μm pixel, this is 0.26%. Compared to the state-of-the-art of 0.95%, this is at least a factor 3 better [5].

The CtC gain versus linearity trade-off can further be influenced by changing the pixel capacitance, which changes the voltage swing on the internal node. For a pixel with 3μm CD, changing the pixel capacitance from 440fF to 220fF increases the CtC gain from 59 μA/pC to 118μA/pC, but decreases the remaining non-linearity from 0.33% to 0.86%. Fig. 16.5.3 shows the measured data.

Finally, we have changed the pixel from a source degenerated topology to a common source topology, as shown in Fig. 16.5.2 [2]. This further improves the CtC gain by a factor 1.40, from 17.6μA/pC to 24.6μA/pC for a pixel with CD of 5μm. The trade-off is once again the non-linearity, which increases from 0.048% to 0.26%. This excellent gain is obtained by combining the common source topology with an amplifier operated in saturation, as shown in Fig. 16.5.4.

The speed limitation of the imager is mainly caused by the speed of the reset TFT. Due to the double correlated sample (CDS) in an active pixel topology, a reset pulse is required between the two subsamples. Propagation of the reset signal is slowed down by the RC of every pixel. R is determined by the technology, and is 27.5Ω/pixel for the 5μm pixel and 49.2Ω/pixel for the 3μm pixel. The capacitance on the line has two components: the gate capacitance of the reset TFT and the wire crossings. We extrapolate from our measurements on larger devices, both capacitances as 7.38fF and 5.15fF in the 3μm design and 13.05fF and 14.30fF in the 5μm design. Our self-aligned IGZO technology greatly improves the state of the art, which is based on back channel etch (BCE) devices with large parasitic capacitances. We estimate that [5] shows a design with a TFT capacitance of 92.0fF and a crossing capacitance of 15.3fF. This implies that we have improved the state-of-the-art with a factor 8.6. In total, we can limit the RC delay per pixel to 0.62ps/pixel corresponding to 0.36μs for an FHD panel line, which is much smaller than the required readout time of 20.8μs for a FHD panel with 50Hz framerate.

Finally, we show a transimpedance readout to limit the cost and noise injection of the readout IC (ROIC), as shown in Fig. 16.5.2. All previous publications use the same readout circuit as the passive pixel sensor (PPS) and integrate the current on a capacitor in the ROIC, see Fig. 16.5.2 [3] [4] [5]. Because of the increased output signal, the required capacitor for an active pixel is much bigger. For the proposed pixel design, a capacitor of 4.7nF was required to accommodate the generated charges with a limited voltage swing of 1.8V (typical ROIC voltage), as can be seen in Fig. 16.5.5. Since the ROIC is a massively parallel device, up to 256 lines per IC, the maximal acceptable capacitor per line is in the order of 10pF per line, several orders of magnitude lower.

The transimpedance readout has another benefit: the input-referred noise of the OTA is no longer amplified toward the output. In an integrating readout, capacitive amplification by the dataline and the integration capacitor can go up to a factor 10 for a dataline capacitance of 100pF, the typical value for BCE flow. Using a transimpedance amplifier, this effect is eliminated. Furthermore, by using the SA technology, the dataline capacitance can be reduced to around 16pF for the 5μm design and 5.6pF for the 3μm design, reducing the overall noise.

A concluding table and comparison with previous works is given in Fig. 16.5.6. Summarized, we show high-performance thin-film pixel on foil with a charge-to-current gain of 59μA/pC, a remaining non-linearity after quadratic calibration of 0.33%, a resolution of 256ppi and capable of FHD with 50Hz framerate. Additionally, we demonstrate a transimpedance approach for the readout IC in order to reduce the integration cost by eliminating the integrating capacitor, while also decreasing the noise from the readout IC.

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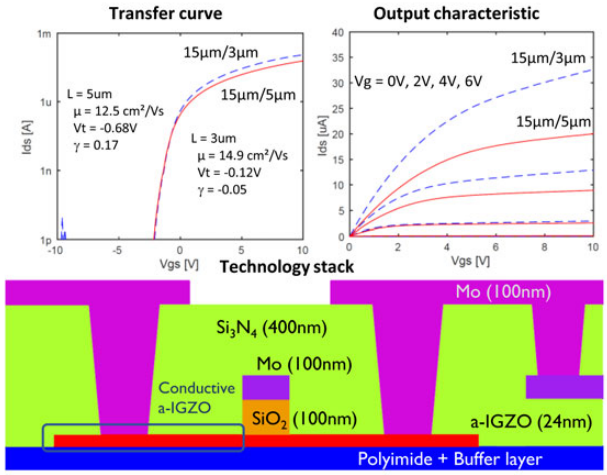

Figure 16.5.1: Technology: device cross section and TFT characteristic. This is a self aligned process, with decreased dataline capacitance, reducing the requirements for readout. Channel lengths down to 3µm were used. More process details can be found in [1].

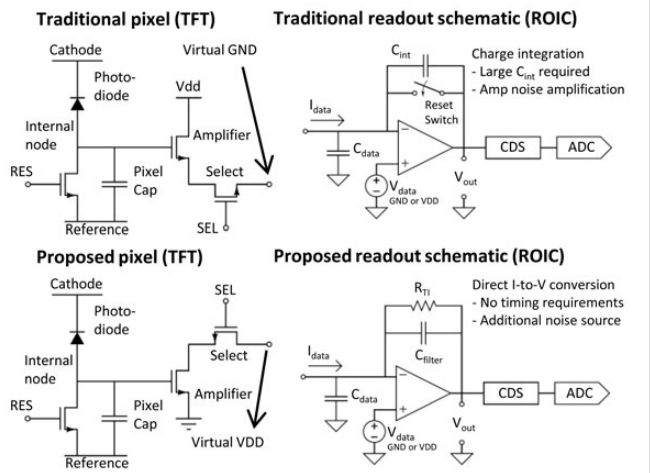

Figure 16.5.2: Schematics for traditional and proposed pixel and readout schemes. Placing the select TFT on the drain side of the amplifier avoids degeneration. Using a transimpedance amplifier in the readout decreases capacitor size for an integrated solution.

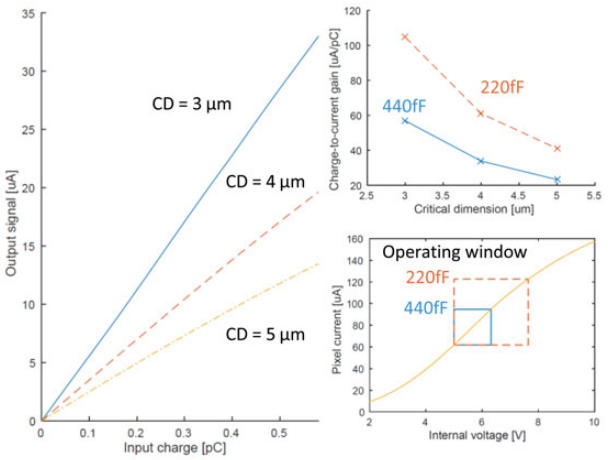

Figure 16.5.3: a. measured pixel performance for different channel lengths. b. effect of channel length scaling and the integration capacitor on charge-to-current gain. c. characterized pixel (3um) with indication of the effect of the pixel capacitor.

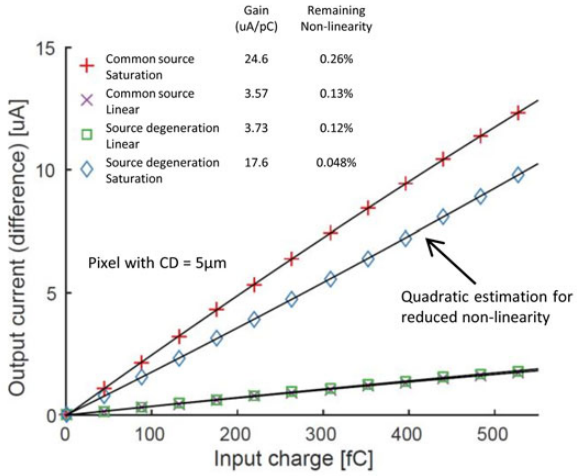

Figure 16.5.4: Performance of internal operation. Comparison between the topologies from figure 2, and the operating regime of the amplifier transistor. Using the transistor as a standard common source amplifier in saturation mode means most gain, but also least linearity.

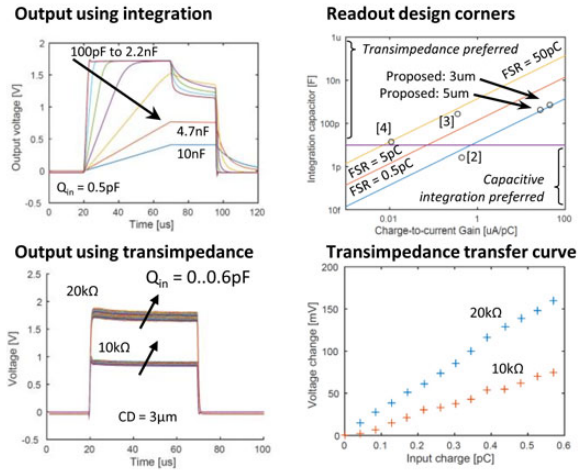

Figure 16.5.5: Readout performance. Fig 5a shows the saturation occurs at capacitors below 4.7nF. Fig 5b shows the required capacitor depending on CtC gain and FSR. Fig 5c shows the response for the trans-impedance approach. Fig 5d shows the input-output curve, measured with an oscilloscope.

	This work		Zhang et al. [1]	Tedde et al. [2]	Karim et al. [3]
Technology	a-IGZO, Self-Aligned		a-IGZO, BCE	a-Si:H, BCE	a-Si:H
Critical dimension	3µm	5µm	4µm	*4µm*	25µm
Pixel pitch	100µm (254 ppi)	100µm (254 ppi)	> 135µm (< 195 ppi)	150µm (169 ppi)	250µm (102 ppi)
Charge-to-current gain	59µA/pC	27µA/pC	*0.011µA/pC*	*0.35µA/pC*	*0.43µA/pC*
Reset load (speed)	6µm/2µm	6µm/5µm	30µm/10µm	30µm/10µm	60µm/25µm
Operating principle	Common source, saturation		Source degen., linear	Source degen., saturation	Source degen., saturation
Readout topology	Transimpedance amplifier		Current integration (C_{FB} = 100pF)	Current integration (C_{FB} = 100pF)	Current integration (C_{FB} = 10pF)
Remaining non-linearity after quadratic calibration	0.33% FSR = 0.58pC	0.26% FSR = 0.58pC	*0.95% FSR = 46pC*	*2.08% FSR = 29pC*	*1.77% FSR = 0.22 pC*

Figure 16.5.6: Comparison table. Numbers in italic are extracted by fitting the figures given in the referenced paper.

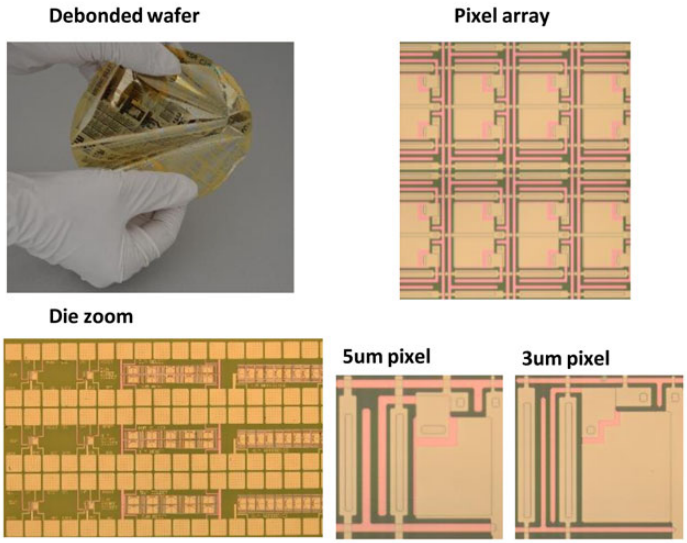

Figure 16.5.7: Die micrograph.

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